Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-10 (cancelled).

11 (currently amended): A chip-packaging with bonding options connected to a package substrate, comprising:

[[a]] the package substrate connected to either a high voltage or a low voltage;

a chip mounted on the package substrate, the chip comprising a plurality of bonding option units, each bonding option unit comprising a bonding pad ~~bonding pads, a first bonding pad directly contacting the package substrate~~; and

a plurality of first lead frames, each bonding pad of the chip having a corresponding first lead frame, the first lead frames being connected to either a high voltage or a low voltage, wherein the voltage level of the first lead frames is the logical opposite of the voltage level of the package substrate;

wherein each bonding pad is selectively connected to the package substrate or the corresponding first lead frame for providing an appropriate voltage to the corresponding bonding option unit.

~~a first lead frame connected to a second bonding pad through a first pin of the chip; and~~

~~a second lead frame connected to a third bonding pad through a second pin of the chip for receiving input signals to control the voltage level of the second pin.~~

12-18 (cancelled).

19 (currently amended): A method of packaging a chip having a bonding option connected to a package substrate, comprising:

providing the package substrate;

connecting the package substrate to either a high voltage or a low voltage;

mounting the chip on the package substrate, the chip comprising a plurality of bonding option units, each bonding option unit comprising a bonding pad ~~bonding pads~~;

providing a plurality of first lead frames, each bonding pad of the chip having a corresponding first lead frame, the first lead frames being connected to either a high voltage or a low voltage, wherein the voltage level of the first lead frames is the logical opposite of the voltage level of the package substrate; and

connecting each bonding pad to either the package substrate or the corresponding first lead frame for providing an appropriate voltage to the corresponding bonding option unit.

~~connecting a first bonding pad directly to the package substrate;~~

~~connecting a second bonding pad to a first lead frame through a first pin of the chip;~~

~~connecting a third bonding pad to a second lead frame through a second pin of the chip; and~~

~~receiving input signals through the second lead frame for controlling the voltage level of the second pin~~.

20-32 (cancelled).

33 (new): The chip-packaging of claim 11, further comprising a plurality of second lead frames, each bonding pad of the chip having a corresponding second lead frame, wherein the second lead frames are used for inputting or outputting

signals to the corresponding bonding pad, and each bonding pad is selectively connected to the package substrate, the corresponding first lead frame, or the corresponding second lead frame.

34 (new): The method of claim 19, further comprising providing a plurality of second lead frames, each bonding pad of the chip having a corresponding second lead frame, wherein the second lead frames are used for inputting or outputting signals to the corresponding bonding pad, and each bonding pad is selectively connected to the package substrate, the corresponding first lead frame, or the corresponding second lead frame.